REMARKS

This Amendment is supplemental to the Amendment filed April 26, 2010, and amends claim 19 for a typographical error. The following Remarks have also been revised accordingly. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claims 1-4 were rejected under 35 USC §103(a) as obvious over the combination of *Hirota* (JP 06-268162 A) in view of *Jeng et al.* (US 6,136,643). Please note that the Office Action refers to the primary reference as Yoshihiro, but this appears to be a given name, and Hirota the surname. This rejection is respectfully traversed.

Claim 1 as presently amended clarifies that the first device formation region is isolated by a device isolation portion having an STI structure, as well as to clarify that the device isolation portion includes, at a boundary between the first region and the second region, the STI structure and the LOCOS oxide film. The STI structure is in contact with the first region, while the LOCOS oxide film is in contact with the second region. Such a structure is shown in FIG. 1 of the present application as originally filed, when viewing the boundary portion of the first region **50** and the second region **70**.

Claim 1 therefore recites "a first region defined on the semiconductor substrate and having a first device formation region isolated by a device isolation portion having an STI structure formed by filling an insulator in a trench formed in

the semiconductor substrate, wherein a surface of the insulator of the STI structure and a surface of the semiconductor substrate are both arranged in a common plane" and wherein "the device isolation portion includes, at a boundary between the first region and the second region, the STI structure in contact with the first region and the LOCOS oxide film in contact with the second region, and *the insulator of the STI structure and the LOCOS oxide film are continuous at the boundary between the first region and the second region*".

Hirota discloses a semiconductor device having an ordinary-breakdown-strength MOS transistor **30** and a high-breakdown-strength MOS transistor **11** both formed on a semiconductor substrate **10**. However, a LOCOS isolation structure using a field oxide film **33** is applied to both the regions around the ordinary-breakdown-strength MOS transistor **30** and around the high-breakdown-strength MOS transistor **11**.

According to the present invention, on the other hand, an STI (Shallow Trench Isolation) structure is adopted for the first region including the device with the lower breakdown voltage, while a LOCOS structure is adopted for the second region including the device having the higher breakdown voltage. See the present specification as filed, e.g. ¶¶[0036] and [0069]:

> **[0036]** With this arrangement, so-called shallow trench isolation (STI) is employed for the device isolation in the first region formed with the first device of the lower breakdown voltage, so that the microminiaturization of the structure in the first region can be advantageously achieved. On the other hand, the second device of the higher breakdown voltage formed in the second region has the drift drain

structure with the LOCOS oxide film provided at the edge of the gate electrode, so that the problem of the concentration of the electric field can be suppressed which may otherwise occur when a thick insulation film of an STI portion is disposed on the edge of the gate electrode. Thus, the second device has a sufficient breakdown voltage.

[0039] The lower breakdown voltage transistors **51** formed in the first region **50** are respectively disposed in device formation regions **53** isolated by a shallow trench isolation (STI) portion **52** formed in a surface of the silicon substrate **40**. The STI portion **52** is formed by filling silicon oxide **55** in a shallow trench **54** (e.g, having a depth of about 4000Å) formed in the surface of the semiconductor substrate **40**.

Thus, in the present invention, the surface of the insulator of the STI structure and the surface of the semiconductor substrate are in the same plane.

The structure of the device according to *Hirota* is shown in Drawing 1 thereof, from which it is apparent that the field oxide film **33** is not in the same plane as a surface of the substrate, but instead stands proud therefrom, i.e. the field oxide film **33** does not have a surface in a common plane with a surface of the substrate. This follows directly because the field oxide film **33** has been made by local oxidation, i.e. by a LOCOS process, and not by filling a trench, whereas in the present invention the device isolation portion is made by filling a trench until it is flush with the substrate.

Hirota therefore fails to teach or suggest that "a surface of the insulator of the STI structure and a surface of the semiconductor substrate are both arranged in a common plane" as recited in claim 1.

No STI structure is shown in anywhere in *Hirota*, which therefore fails to disclose a device isolation portion having an STI structure as well as a LOCOS

oxide film at a boundary between a first region and a second region. *Hirota* therefore naturally fails to disclose that an STI structure is in contact with a first region in which relatively low breakdown voltage device is formed, while a LOCOS oxide film is in contact with the second region in which a higher breakdown voltage device is formed. A person of ordinary skill in the art would consider an STI structure and a LOCOS structure to be different structures that are clearly distinguishable from each other.

Hirota (Yoshihiro) thus also fails to disclose that "the device isolation portion includes, at a boundary between the first region and the second region, the STI structure in contact with the first region and the LOCOS oxide film in contact with the second region, and *the insulator of the STI structure and the LOCOS oxide film are continuous at the boundary between the first region and the second region*".

The Office Action states on page 3 thereof that *Jeng et al.* discloses "Wherein a surface of the device isolation portion and a surface of the semiconductor substrate are both arranged in a common plane" in column 2, lines 35-46 thereof:

> ... This allows self-aligned contacts to be made with relaxed photolithographic alignment tolerances.
>
> The method begins by providing a semiconductor substrate. Typically the substrate is a P^- doped single-crystal silicon substrate having a <100> crystallographic orientation. Device areas are provided by forming a relatively thick Field OXide (FOX) that surrounds and electrically isolates each device area in and on the substrate. One method of forming the field oxide is by shallow trench

> isolation (STI) in which a shallow trench is etched in the substrate and filled with a silicon oxide (SiO_2) that is made essentially planar with the substrate surface. ...

Thus, *Jeng et al.* discloses an STI structure. However, *Jeng et al.* fails to teach or suggest a structure that includes within it both an STI structure and a LOCOS structure.

Jeng et al. states in column 2, lines 42-46 thereof that "One method of forming the field oxide is by shallow trench isolation (STI) in which a shallow trench is etched in the substrate and filled with a silicon oxide (Si02) that is made essentially planer with the substrate surface". However, *Jeng et al.* fails to disclose that "the device isolation portion includes, at a boundary between the first region and the second region, the STI structure in contact with the first region and the LOCOS oxide film in contact with the second region, and *the insulator of the STI structure and the LOCOS oxide film are continuous at the boundary between the first region and the second region*" as recited in claim 1.

Therefore, *Jeng et al.* fails to remedy the deficiencies of *Hirota*. Therefore, even the combination of the teachings by Yoshihiro and Jeng et al. cannot render the present invention to be obvious for a person having ordinary skill in the, art.

As *Hirota* (Yoshihiro) and *Jeng et al.* both fail to teach or suggest a structure that includes an STI structure in a first region and a LOCOS structure in a second region, they must naturally fail to teach or suggest a structure in which an insulator for the STI structure is continuous with a LOCOS oxide film at a boundary between the first and second regions.

Hence, neither *Hirota* (Yoshihiro) nor *Jeng et al.*, whether taken separately or in combination, teaches or suggests that "the device isolation portion includes, at a boundary between the first region and the second region, the STI structure in contact with the first region and the LOCOS oxide film in contact with the second region, and the insulator of the STI structure and the LOCOS oxide film are continuous at the boundary between the first region and the second region" as recited in claim 1.

Consequently, claim 1 patentably defines over *Hirota* (Yoshihiro) and *Jeng et al.* and is allowable, together with claims 2 and 4 dependent therefrom, and as claim 1 is generic it is respectfully requested that the species of withdrawn claim 3 be rejoined with the species of claims 2 and 4, and claim 3 allowed therewith.

Newly added claims 18 and 19 depend directly or indirectly from claim1 and are therefore allowable for at least the same reasons as claim 1.

New dependent claim 18 further limits claim 1 in that the second region has a plurality of the second device formation regions that are isolated by a second device isolation portion including an STI portion and a LOCOS portion. The STI portion is formed by filling an insulator in a trench formed in the semiconductor substrate, while the LOCOS portion is in contact with the second device.

New dependent claim 19 depends from claim 18, and further limits claim 18 in that the insulator of the STI portion is continuous with the LOCOS portion.

The features recited in claims 18 and 19 are shown in FIG. 1 of the present application as originally filed. In the second region **70**, there are a plurality of

device formation regions **73**. An adjacent pair of the device formation regions **73** are isolated by an STI portion **72** and LOCOS oxide films **84** and **85**. The insulator **75** of the STI portion **22** is continuous with the LOCOS oxide films **84** and **85**. The LOCOS oxide films **84** and **85** are in contact with transistors **71**, respectively.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

No remittance is believed to be due. Should any fee be required, however, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,

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Date

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